Applicant respectfully submits that claim 18 is patentable over Vaartstra in view of Ouellet as there is no disclosure or suggestion in the references of a parallel plate capacitor over a dielectric layer, wherein the parallel plate capacitor extends into and out of a plurality of recesses in the semiconductor layer. Vaartstra teaches a method of forming a film on a semiconductor device using carboxylate complexes. Fig. 1 of Vaartstra shows a memory cell in which a ferroelectric material 11 is formed between two electrodes 12 and 13. The bottom electrode 13 is formed on a silicon-containing layer 14 such as silicon dioxide. While layer 14 extends into recesses in a substrate, as shown in FIG. 1, layer 14 fills the recesses and no part of the capacitor extends into or out of the recesses. The Examiner argues that FIG. 1 of Vaartstra is not drawn to scale and so the capacitor may be extending into and out of recess in a semiconductor. However, in order to properly reject the claims, the prior art must disclose or suggest the claimed invention to one of ordinary skill in the art. While recesses are shown in FIG. 1 of Vaartstra, the recesses are not mentioned in the text of the patent. There is no discussion as to their purpose or depth. As illustrated, the parallel plate capacitor does not extend into and out of recesses in a semiconductor layer and there is no teaching in Vaartstra to suggest modifying a depth of the recess such that a parallel plate capacitor that extends into and out of recesses in a semiconductor layer. Ouellet is added to teach that capacitors are used in memories and analog circuits. Accordingly, Applicant respectfully submits that claim 18 and the claims dependent thereon are patentable over Vaartstra in view of Ouellet.

The Examiner rejected claims 21-22 under 35 U.S.C. § 103(a) as being unpatentable over Vaartstra (U.S. 6,010,969) in view of Ouellet et al. (U.S. 6,268,620) and further in view of Maniar (U.S. 5,185,689).

Applicant respectfully submits that claims 21 and 22 are patentable over the references for the same reasons discussed above relative to claim 18 from which these claims depend. Maniar is added to teach PZT as a capacitor dielectric. There is no disclosure or suggestion in the references of a parallel plate capacitor over a dielectric

layer, wherein the parallel plate capacitor extends into and out of a plurality of recesses in the semiconductor layer.

In light of the above, Applicant respectfully requests withdrawal of the Examiner's rejections and allowance of claims 18-22. If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully submitted,
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